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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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LSI LOGIC CORPORATION
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PATENT LAW DEPARTMENT
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EXAMINER

DUNCAN, MARC M

ART UNIT PAPER NUMBER

2113

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/966,327

Applicant(s)

ALANI ET AL.

Examiner

Marc Duncan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 June 2005.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-3 and 10-19 is/are rejected.
7) ☒ Claim(s) 4-9 and 20 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 20 December 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

Claims 1-3 and 10-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Schenck (6,072,329).

Claims 4-9 and 20 are objected to.

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in the United Kingdom on 4 October 2000. It is noted, however, that applicant has not filed a certified copy of the UK application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 10-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Schenck (6,072,329).

Regarding claim 1:

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Schenck teaches a circuit configured to monitor a plurality of signals for transitions and invert said signals (transmit in complementary state) only when at least a predetermined number of said signals (only transmit in complementary state when more than half of lines are transitioning) transition to a particular logic state (col. 2 lines 16-30 – the signals transition from to either high or low, each of which is a particular logic state).

Schenck teaches a plurality of buffers configured to present said signals on a transmission bus (col. 2 lines 28-30).

Regarding claim 2:

Schenck teaches wherein said particular logic state is one of (i) a high logic state and (ii) a low logic state in col. 2 lines 20-23.

Regarding claim 3:

Schenck teaches wherein said predetermined number of signals is greater than one half of a total number of signals in col. 2 lines 22-24.

Regarding claim 10:

Schenck teaches monitoring signals for transitions (col. 2 lines 16-30).

Schenck teaches inverting said signals only in response (transmit in complementary only when more than half of the signals transition to a high or low state)

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to at least a predetermined number (more than half) of said signals transitioning to a particular logic state (col. 2 lines 16-30 - low or high, each is particular logic state).

Schenck teaches presenting said signals on a transmission bus (col. 2 lines 28-30).

Regarding claim 11:

Schenck teaches wherein said particular logic state is one of (i) a high logic state and (ii) a low logic state in col. 2 lines 20-23.

Regarding claim 12:

Schenck teaches wherein said predetermined number of signals is greater than one half of a total number of said signals in col. 2 lines 22-24.

Regarding claim 13:

Schenck teaches generating a plurality of transition signals each indicating a transition direction of one of said signals (col. 5 lines 16-25).

Schenck teaches generating a flag signal (parity signal) when at least said predetermined number of said transition signals indicate said transition direction is to said particular logic state (col. 4 lines 7-23).

Regarding claim 14:

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Schenck teaches presenting said flag signal on said transmission bus in col. 4 lines 45-53.

Regarding claim 15:

Schenck teaches sampling said signals to present a plurality of sampled signals (col. 4 lines 2-4).

Schenck teaches inverting said signals to present a plurality of inverted signals (col. 6 lines 7-11).

Schenck teaches logical combining said sampled signals and said inverted signals to present said transition signals (col. 4 lines 1-6).

Regarding claim 16:

Schenck teaches storing said signals prior to presenting said signal on said transmission bus in col. 4 lines 33-37.

Regarding claim 17:

Schenck teaches generating a clock signal to control said storing in col. 4 lines 33-37.

Regarding claim 18:

Schenck teaches mean for monitoring signals for transitions (col. 2 lines 16-30).

Schenck teaches means for inverting said signals only in response (transmit in complementary only when more than half of the signals transition to a high or low state) to at least a predetermined number (more than half) of said signals transitioning in a predetermined direction (col. 2 lines 16-30 – low to high and high to low are both transitions in predetermined directions).

Schenck teaches means presenting said signals on a transmission bus (col. 2 lines 28-30).

Regarding claim 19:

Schenck teaches wherein said predetermined direction is one of (i) a high to low direction and (ii) a low to high direction in col. 2 lines 20-23.

Allowable Subject Matter

Claims 4-9 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 6/2/05 have been fully considered but they are not persuasive.

Applicant argues, on pages 9-11, that the Schenck reference does not anticipate claim 18 because claim 18 recites inverting only in response to a predetermined number

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of signal transitioning in a predetermined direction. The examiner respectfully disagrees. It is the examiner's position that a high to low transition and a low to high transition are each transitions in a predetermined direction, i.e. high to low or low to high. Either direction transition is read on by the claim language of claim 18. Schenck further transitions only in response to one of the direction changes. Applicant appears to be interpreting the claim to dictate transitioning only in a **single** predetermined direction. The examiner, however, disagrees with that interpretation and urges applicant to put such language into the claim if that is in fact what applicant intends.

Applicant argues, on pages 12-13, that Schenck does not anticipate claim 19 because claim 19 states one of a high to low or a low to high transition. Schenck teaches each of the transitions and thus clearly anticipates the case where one of the transitions is necessary. If applicant would like the directions to be considered as being in mutually exclusive cases, the examiner urges applicant to make that clear in the language of the claim.

Applicant argues, on page 14, essentially the same argument given concerning claims 18 and 19 with respect to claims 1 and 2. The sole difference in the arguments concerning claims 1 and 2 is that the predetermined direction has been changed to a particular logic state. Schenck clearly teaches a predetermined logic state to which the signal is transitioned. The signal is transitioned to either logic state high or logic state low. Each of these is a particular logic state and Schenck thus reads on the logic state whether said state is the high logic state or the low logic state. Again, applicant appears to be interpreting the claim to dictate transitioning only to a **single** predetermined logic

state. The examiner, however, disagrees with that interpretation and strongly urges applicant to put such language into the claim if that is in fact what applicant intends.

The examiner has removed the rejections to claims 4, 6 and 9, thus rendering moot the arguments concerning said rejections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc Duncan whose telephone number is 571-272-3646. The examiner can normally be reached on M-F 9:00-5:00.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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